REMARKS

The Office Action of **May 14, 2002**, has been received and its contents carefully noted. Applicant respectfully submits that this response is timely filed and fully responsive to the Office Action.

Claims 1-12 and 34-42 were pending in the present application prior to the aforementioned amendment. By the above actions, claims 1 and 3 are amended, and new claims 43-74 added. Accordingly, claims 1-12 and 34-74 are currently pending in the present application and, at least for the reasons set forth below, are believed to be in condition for allowance.

A. Objection to the Specification

The Examiner objects to the specification as lacking a descriptive title of the invention. In response thereto, the title of the invention is substituted for one which is more indicative of the invention to which the claims are directed. Notably, the new title of the invention is "SEMICONDUCTOR DEVICE INCLUDING NONVOLATILE MEMORY ARRAY."

B. 35 U.S.C. §103 Rejection

Claims 1-12 and 34-42 stand rejected under 35 U.S.C. §103(a) as unpatentable over JP Patent No. 11-154714 to Yamazaki et al. (Hereinafter "Yamazaki") in view of U.S. Patent No. 5,656,845 to Akbar. It is respectfully contended that the claimed invention as presently amended

clearly defines over the proposed combination of Yamazaki and Akbar for at least the following reasons.

The claimed invention is directed generally to nonvolatile memory including, *inter alia*, a memory cell array including a plurality of memory cells being formed in a matrix, each of the memory cells including a memory thin film transistor and a switching thin film transistor.

Moreover, the nonvolatile memory in accordance with the rejected claims as presently amended requires:

(1) a first semiconductor active layer of the memory thin film transistor connected to a third signal line,

(2) a second semiconductor active layer of the switching thin film transistor connected to a fourth signal line,

(3) the second signal line be formed between the semiconductor active layers and the first signal line,

(4) the first signal line and the second signal line be perpendicular to the third signal line and the fourth signal line,

(5) formation of the floating gate electrode of the memory thin film transistor, the gate electrode of the switching thin film transistor, and the first signal line and the second signal line of a same layer, and wiring of the memory thin film transistor, the third signal line and the fourth signal line are formed of a same layer.

1. The Proposed Yamazaki Modification Fails to Disclose the Claimed Invention

Applicant respectfully contends that Yamazaki, either alone or in combination with Akbar, clearly fails to expressly teach, disclose or inherently suggest each and every claim limitation of the prevent invention as presently amended. In particular, the switching TFT (Tr2) and memory TFT (Tr1) of the memory cell array disclosed by Yamazaki lacks the necessary structure recited in the claimed invention. For instance, the memory TFT (Tr1) lacks a first semiconductor active layer that is connected to a third signal line while the switching TFT (Tr2) lacks a second semiconductor active layer that is connected to a fourth signal line. The memory cell array of Yamazaki also lacks a floating gate electrode of the memory thin film transistor, a gate electrode of the switching thin film transistor, and a first signal line and a second signal line that are formed of a same layer. Yamazaki also lacks a device whereby a wiring of the memory thin film transistor, the third signal line and the fourth signal line are formed of a same layer.

Moreover, the secondary reference Akbar also fails to disclose the aforementioned features that are required by the claimed invention as presently amended. Therefore, a *prima facie* case of obvious cannot stand against claims 1-12 and 34-42 even when Yamazaki and Akbar are combined. In view of the foregoing remarks, reconsideration and withdrawal of the rejection is earnestly solicited.

C. Non-Statutory Double Patenting Rejections

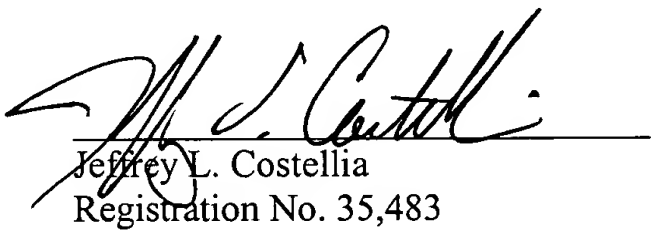
The Examiner provisionally rejects claims 1-12 and 34-42 under the judicially created doctrine of obviousness-type double patenting over claims 1-12 of copending U.S. Application No. 09/156,913 and also over claims 1-30 of copending U.S. Application No. 09/988,729 in view

of Akbar. Applicant respectfully request that the Examiner hold these rejections in abeyance until an indication of allowance of the claims over the prior art has been indicated.

Conclusion

Accordingly, Applicant respectively submits that the pending claims are in proper condition for allowance and reconsideration and withdrawal of the pending rejections are requested. If the Examiner believes further discussions with Applicant's representative would be beneficial in this case, he is invited to contact the undersigned.

Respectfully submitted,



Jeffrey L. Costellia
Registration No. 35,483

NIXON PEABODY LLP
8180 Greensboro Drive, Suite 800
McLean, VA 22102
(703) 770-9300

JLC/TAV

MARKED UP VERSION OF AMENDED CLAIMS

1. (Amended) A nonvolatile memory comprising:

memory cell array including a plurality of memory cells being formed in a matrix[;], each of the memory cells including a memory thin film transistor and a switching thin film transistor,

wherein said memory thin film transistor comprises:

a first semiconductor active layer over an insulating substrate;

a first insulating film;

a floating gate electrode;

a second insulating film;

a control gate electrode;

a wiring for connecting the control gate electrode with a first signal line,

wherein said switching thin film transistor [including] comprises:

a second semiconductor active layer over the insulating substrate;

a gate insulating film;

a gate electrode connected to a second signal line,

wherein the memory thin film transistor and the switching thin film transistor are integrally formed over the insulating substrate,

wherein the first semiconductor active layer of the memory thin film transistor and the second semiconductor active layer are [continuously formed] in a common semiconductor island,

wherein a first thickness of the first semiconductor active layer of the memory thin film transistor is thinner than a second thickness of the second semiconductor active layer of the switching thin film transistor,

wherein the first semiconductor active layer of the memory thin film transistor is connected to a third signal line,

wherein the second semiconductor active layer of the switching thin film transistor is connected to a fourth signal line,

wherein the second signal line is formed between the semiconductor active layers and the first signal line,

wherein the first signal line and the second signal line are perpendicular to the third signal line and the fourth signal line,

wherein the floating gate electrode of the memory thin film transistor, the gate electrode of the switching thin film transistor, the first signal line and the second signal line are formed of a same layer, and

wherein the wiring of the memory thin film transistor, the third signal line and the fourth signal line are formed of a same layer.

3. (Amended) A nonvolatile memory comprising:

a memory cell array including a plurality of memory cells being formed in a matrix[;], each of the memory cells including a memory thin film transistor and a switching thin film transistor,

wherein said memory thin film transistor comprises:

a first semiconductor active layer over an insulating substrate;

a first insulating film;

a floating gate electrode;

a second insulating film;

a control gate electrode;

a wiring for connecting the control gate electrode with a first signal line,

wherein said switching thin film transistor comprises:

a second semiconductor active layer over the insulating substrate;

a gate insulating film;

a gate electrode connected to a second signal line,

wherein the memory thin film transistor and the switching thin film transistor are integrally formed over the insulating substrate,

wherein the first semiconductor active layer of the memory thin film transistor and the second semiconductor active layer are [continuously formed] in a common semiconductor island,

wherein a first thickness of the first semiconductor active layer of the memory thin film transistor is in a range of 1-100 nm while a second thickness of the second semiconductor active layer of the switching thin film transistor is in a range of 1-150 nm,

wherein the first semiconductor active layer of the memory thin film transistor is connected to a third signal line,

wherein the second semiconductor active layer of the switching thin film transistor is connected to a fourth signal line,

wherein the second signal line is formed between the semiconductor active layers and the first signal line,

wherein the first signal line and the second signal line are perpendicular to the third signal line and the fourth signal line,

wherein the floating gate electrode of the memory thin film transistor, the gate electrode of the switching thin film transistor, the first signal line and the second signal line are formed of a same layer, and

wherein the wiring of the memory thin film transistor, the third signal line and the fourth signal line are formed of a same layer.